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Poor Man's Intro to Bonding

KiCon Asia 2025

Open Skunkforce e.V.

CONNECTING ENGINEERS AND UNIVERSITIES

RUNNING CONFERENCES

SINCE 2021

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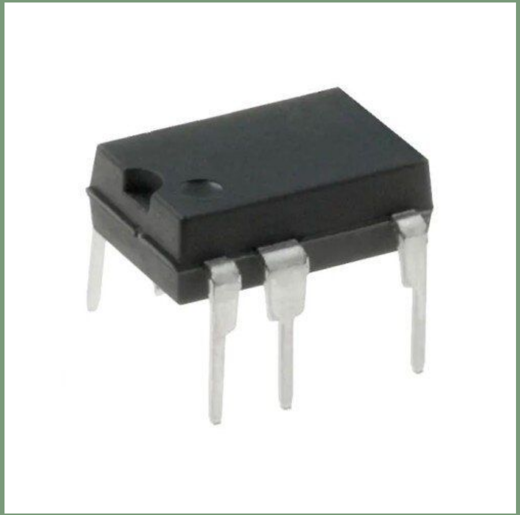

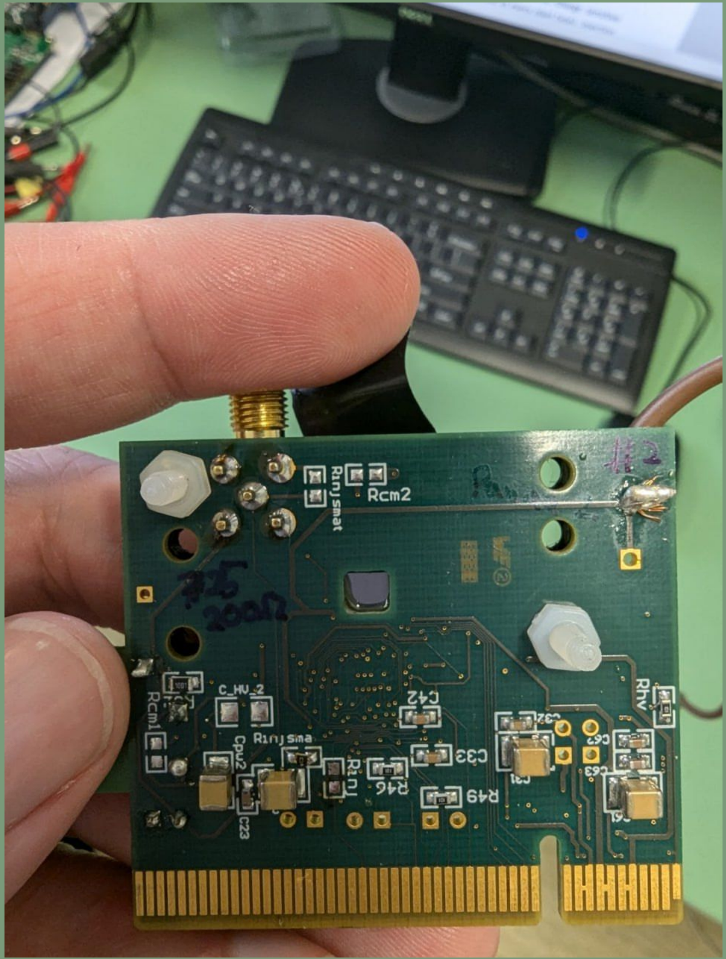

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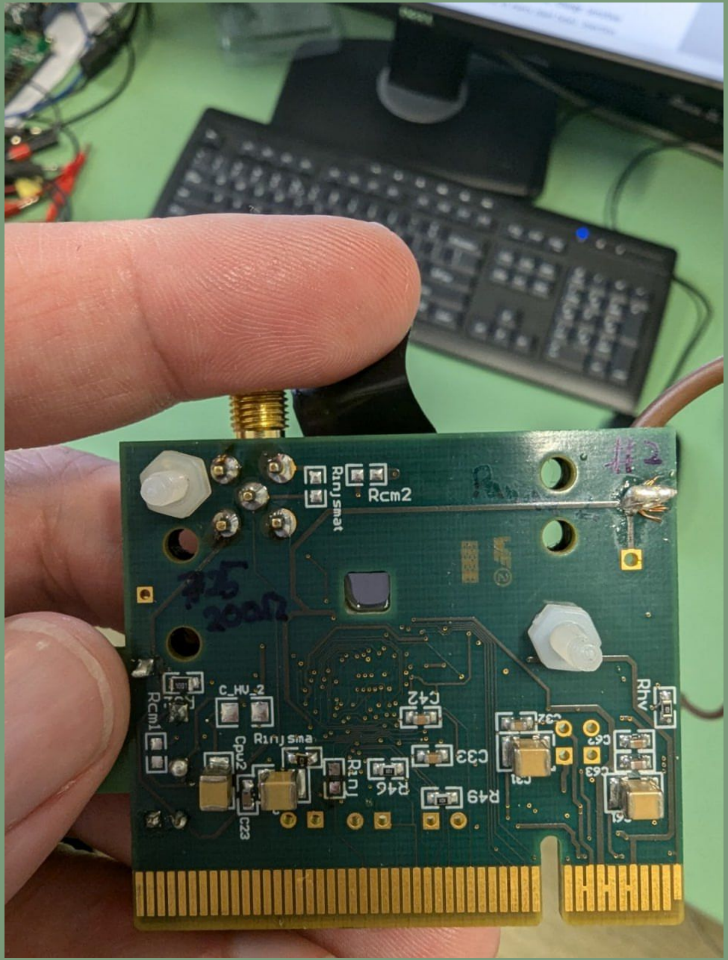

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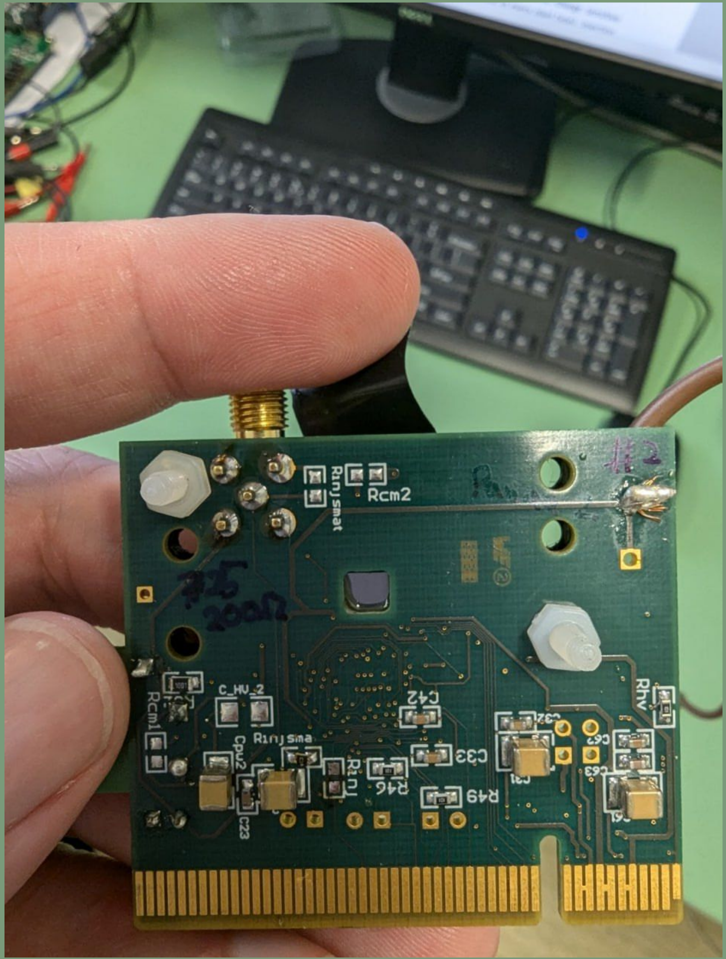

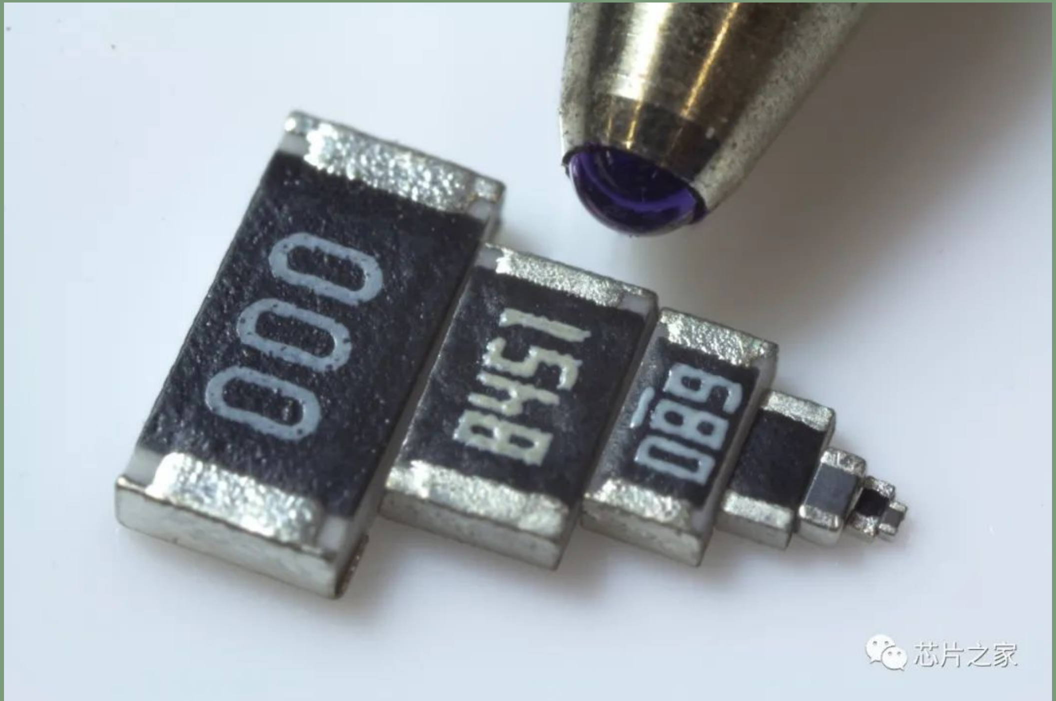
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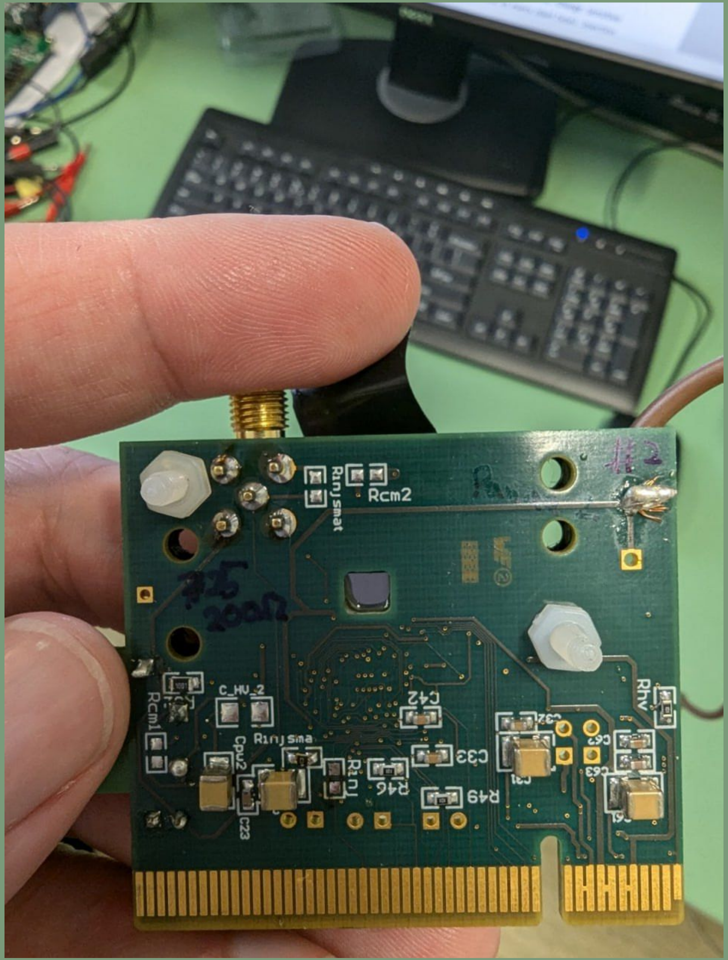
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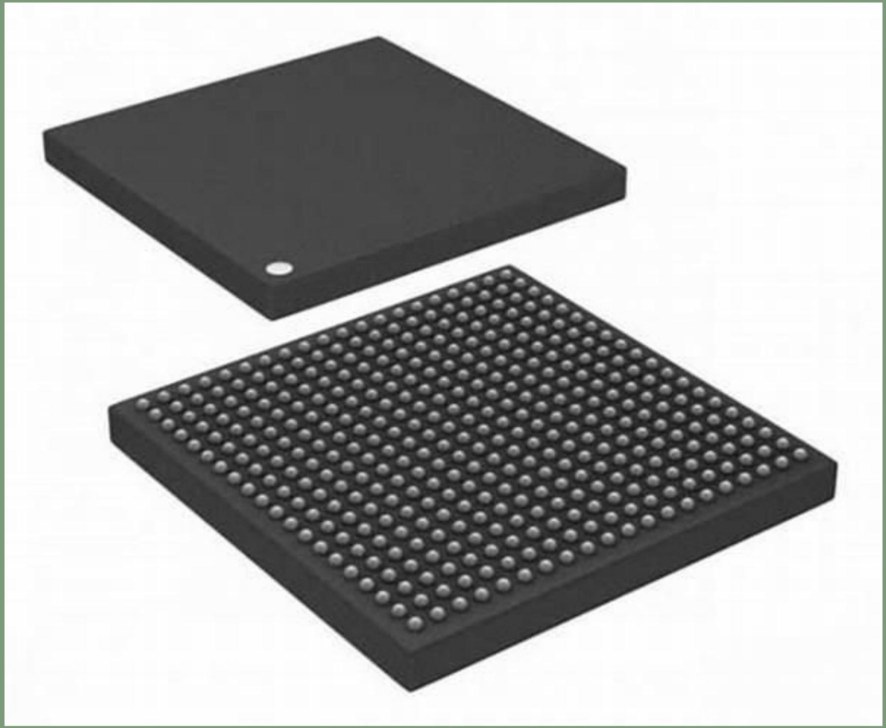

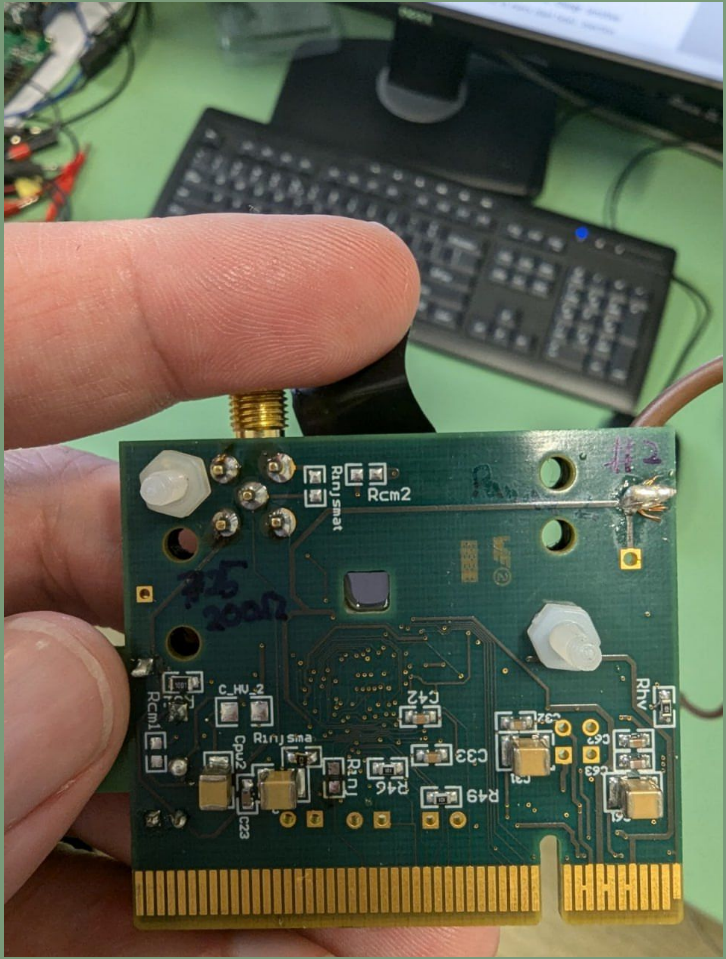

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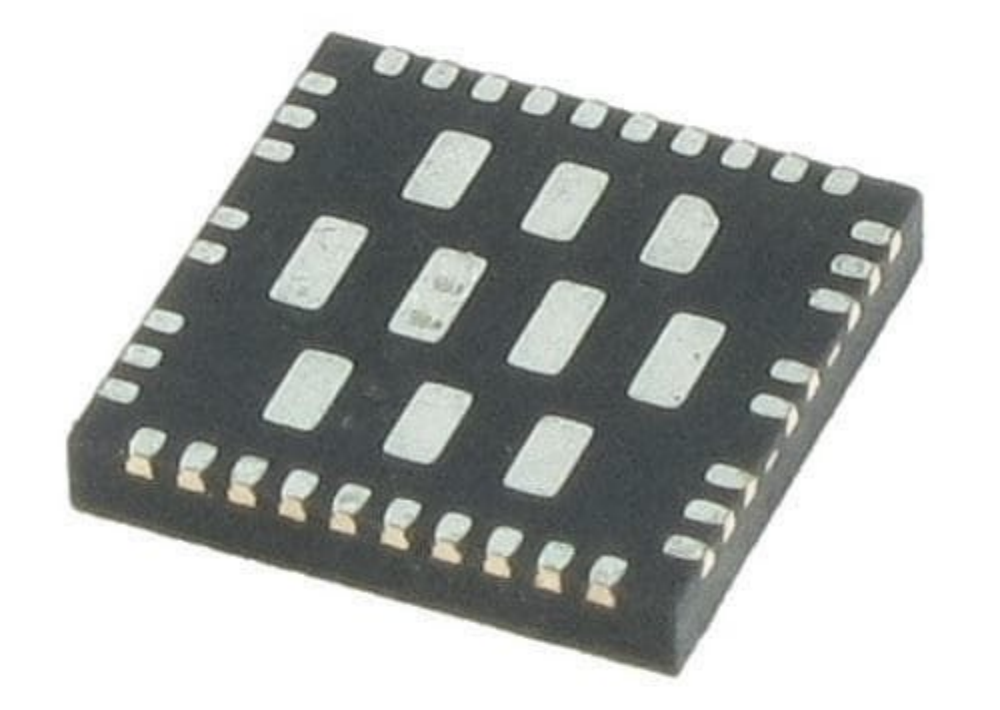

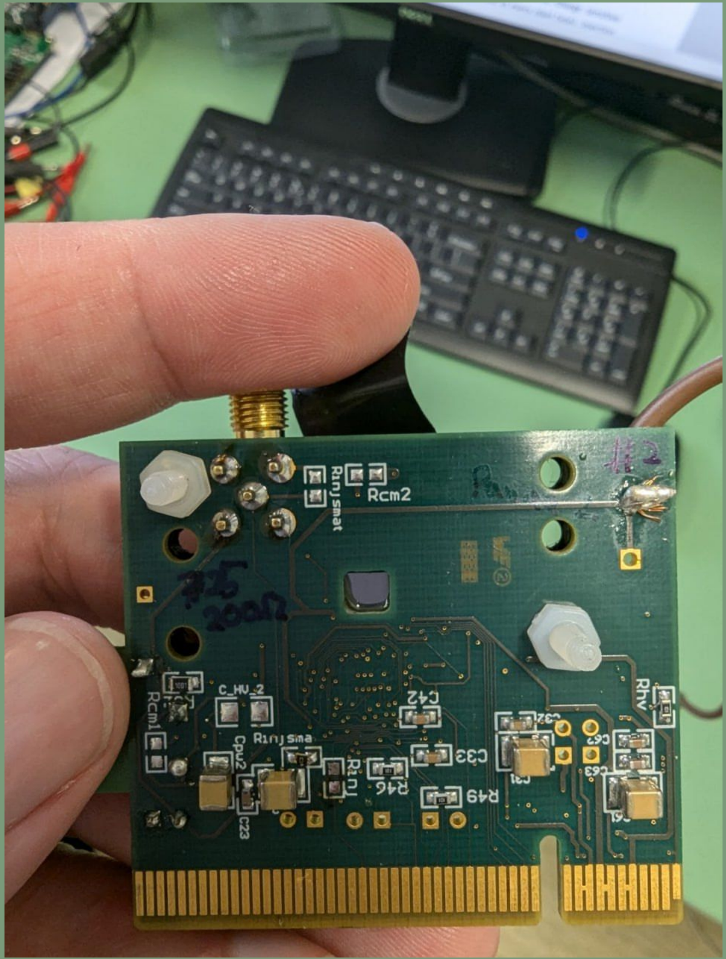

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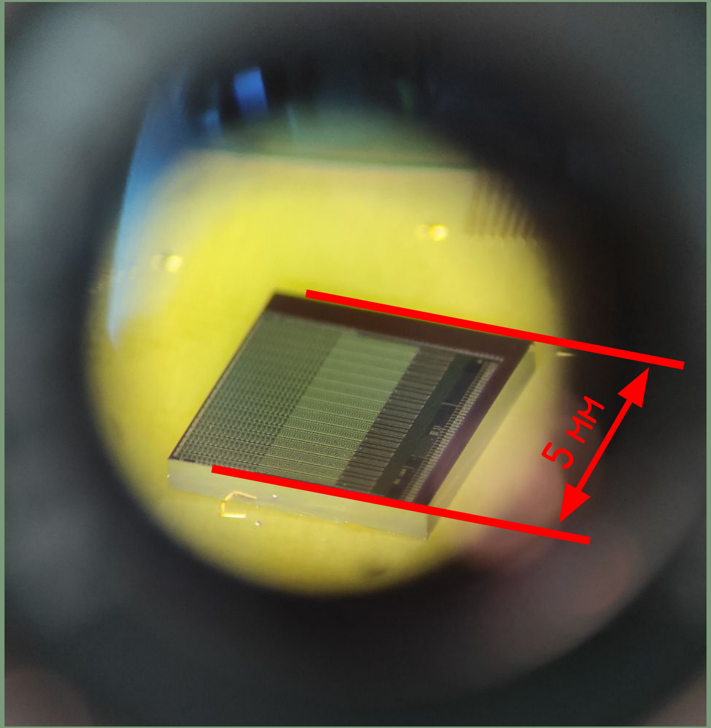

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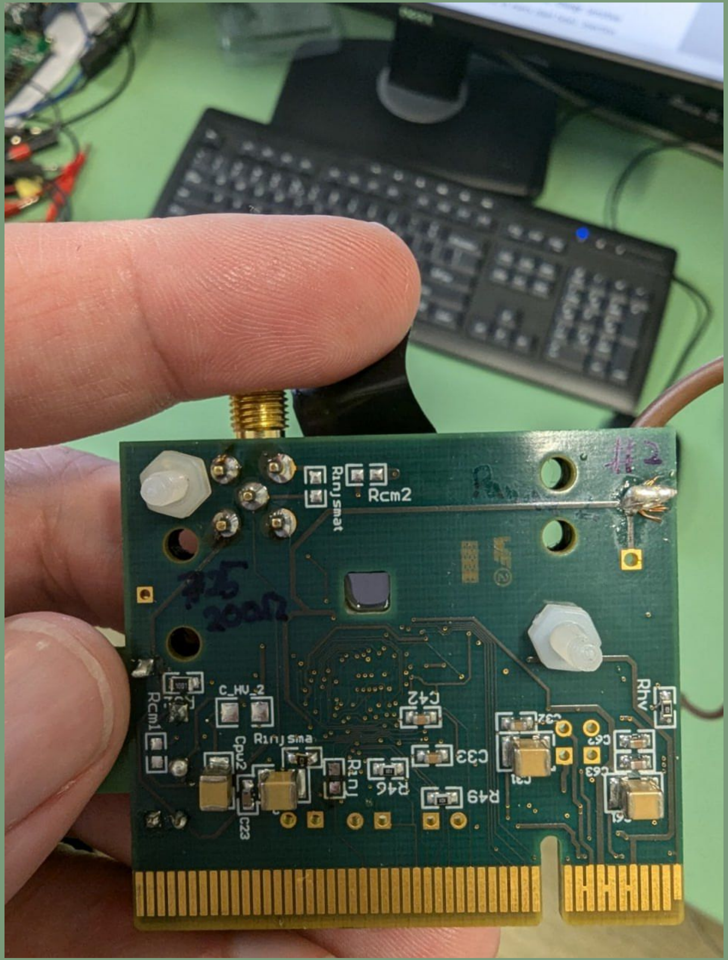

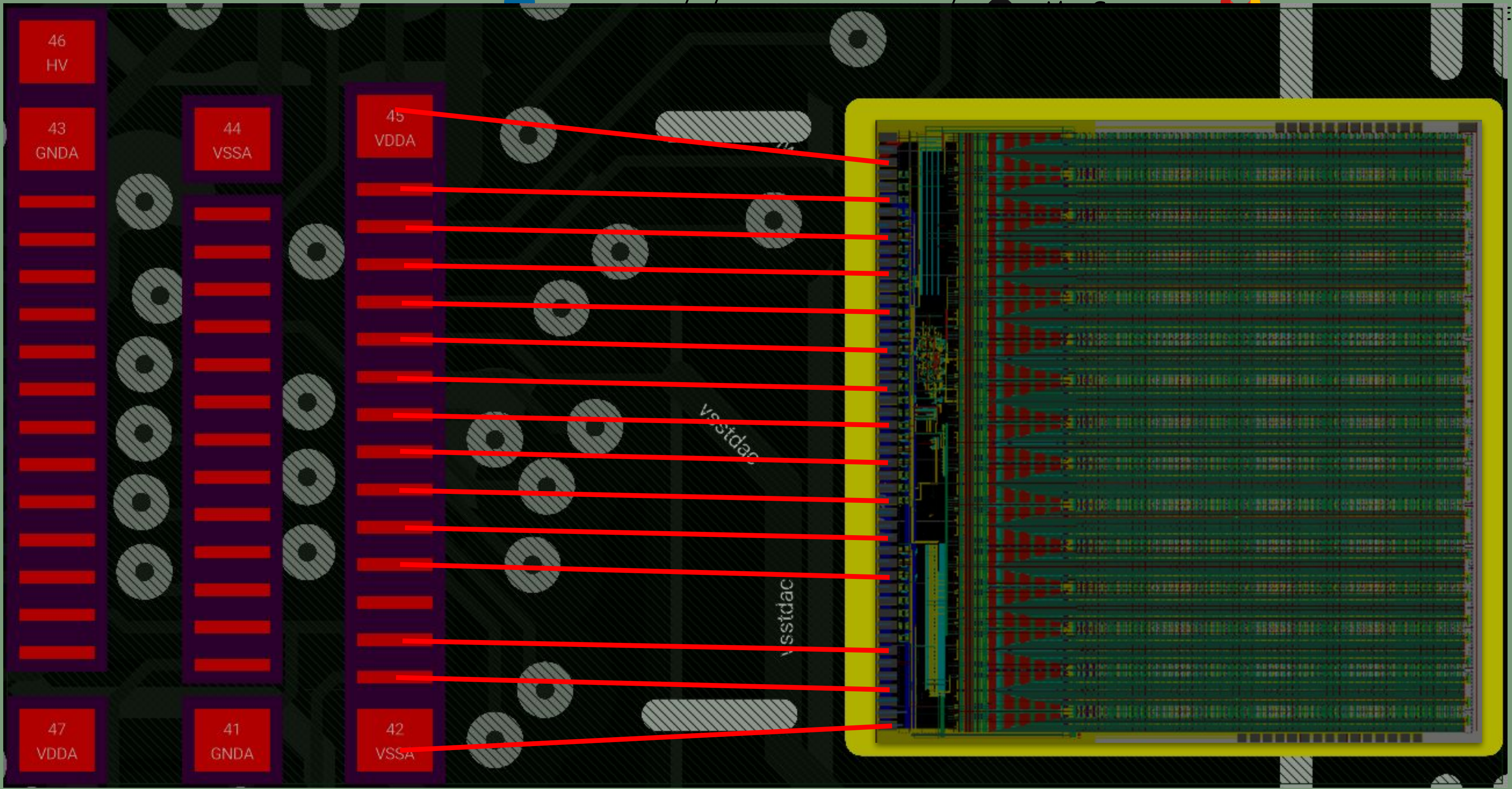
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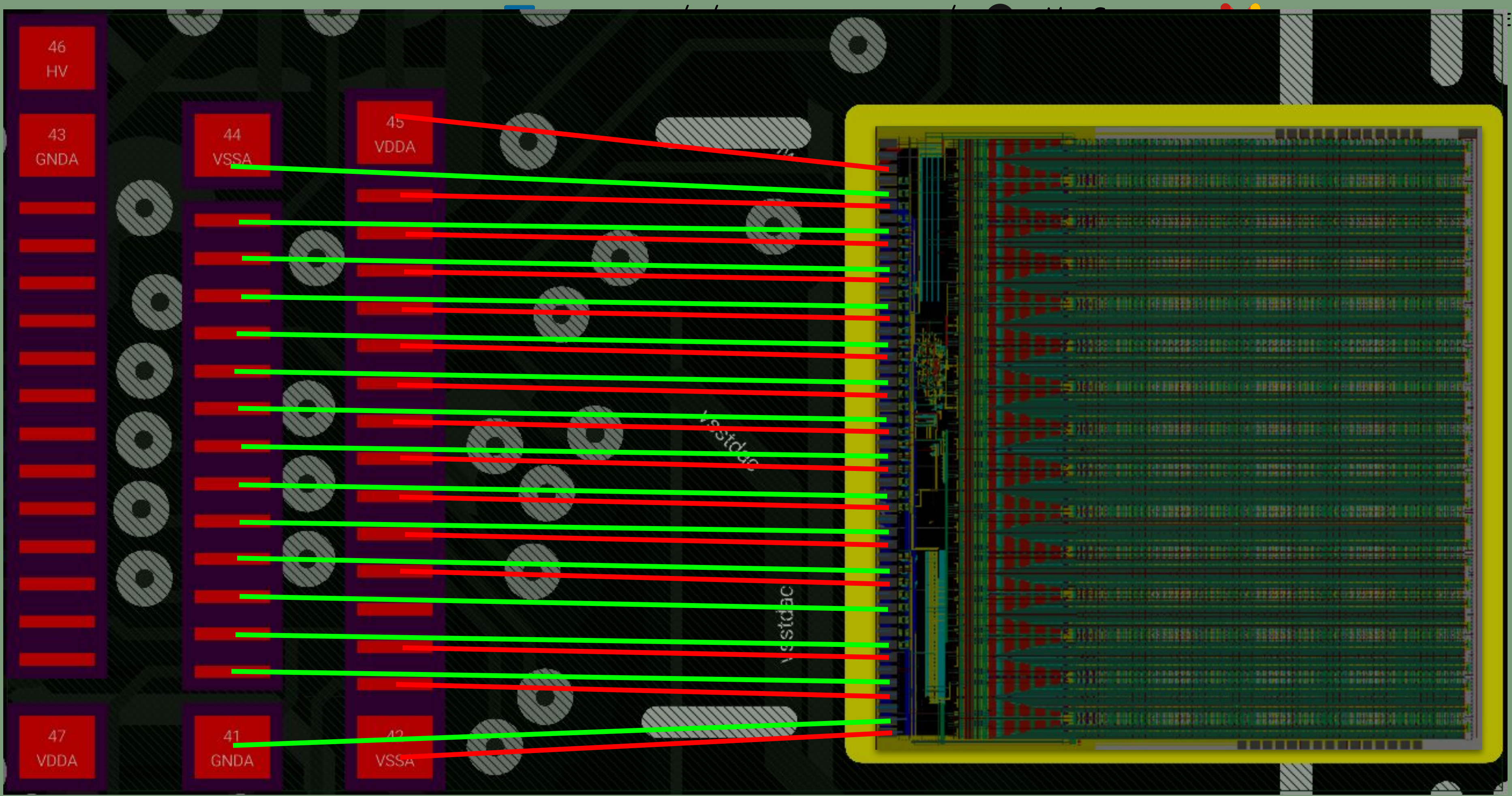
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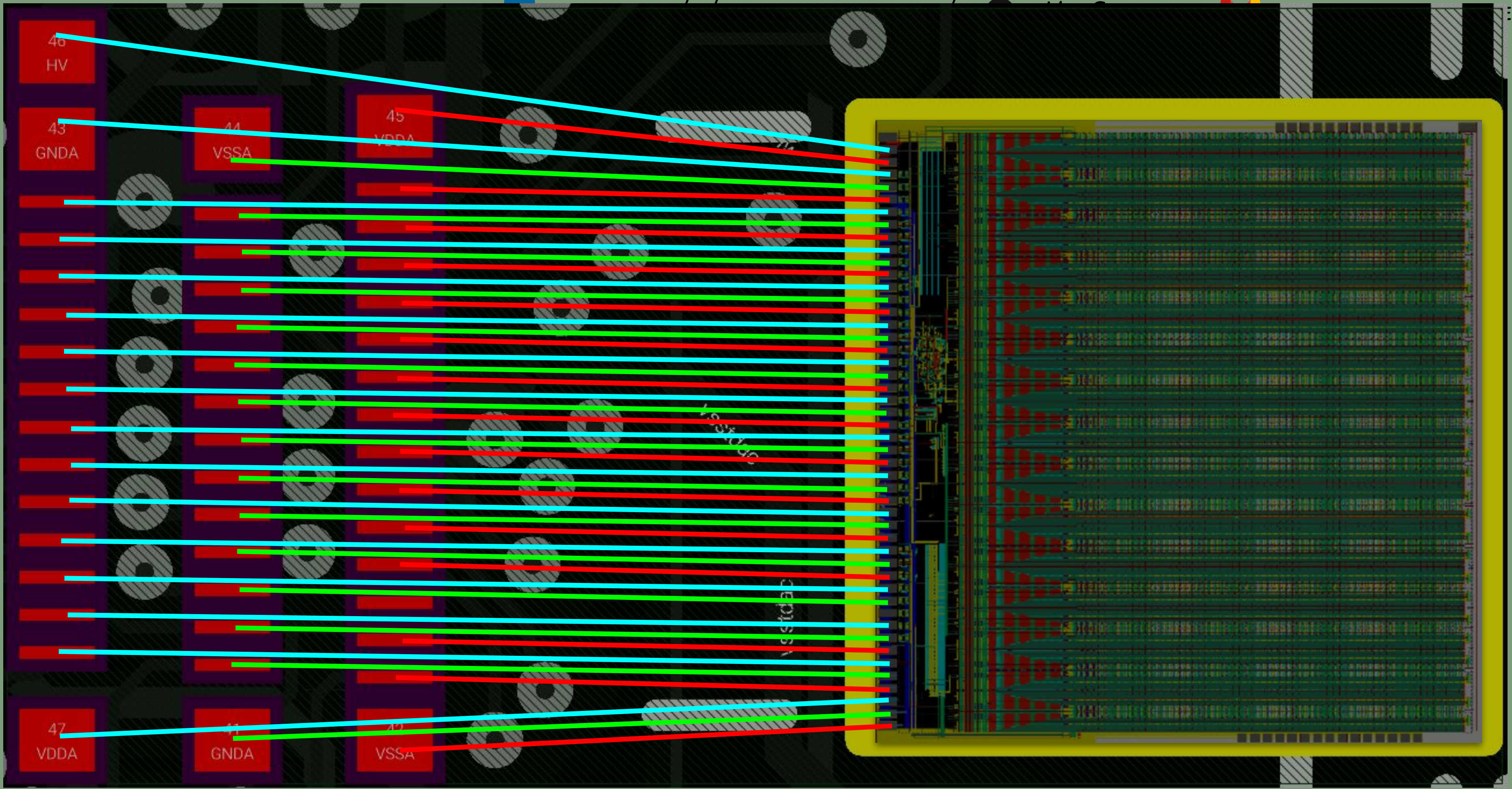
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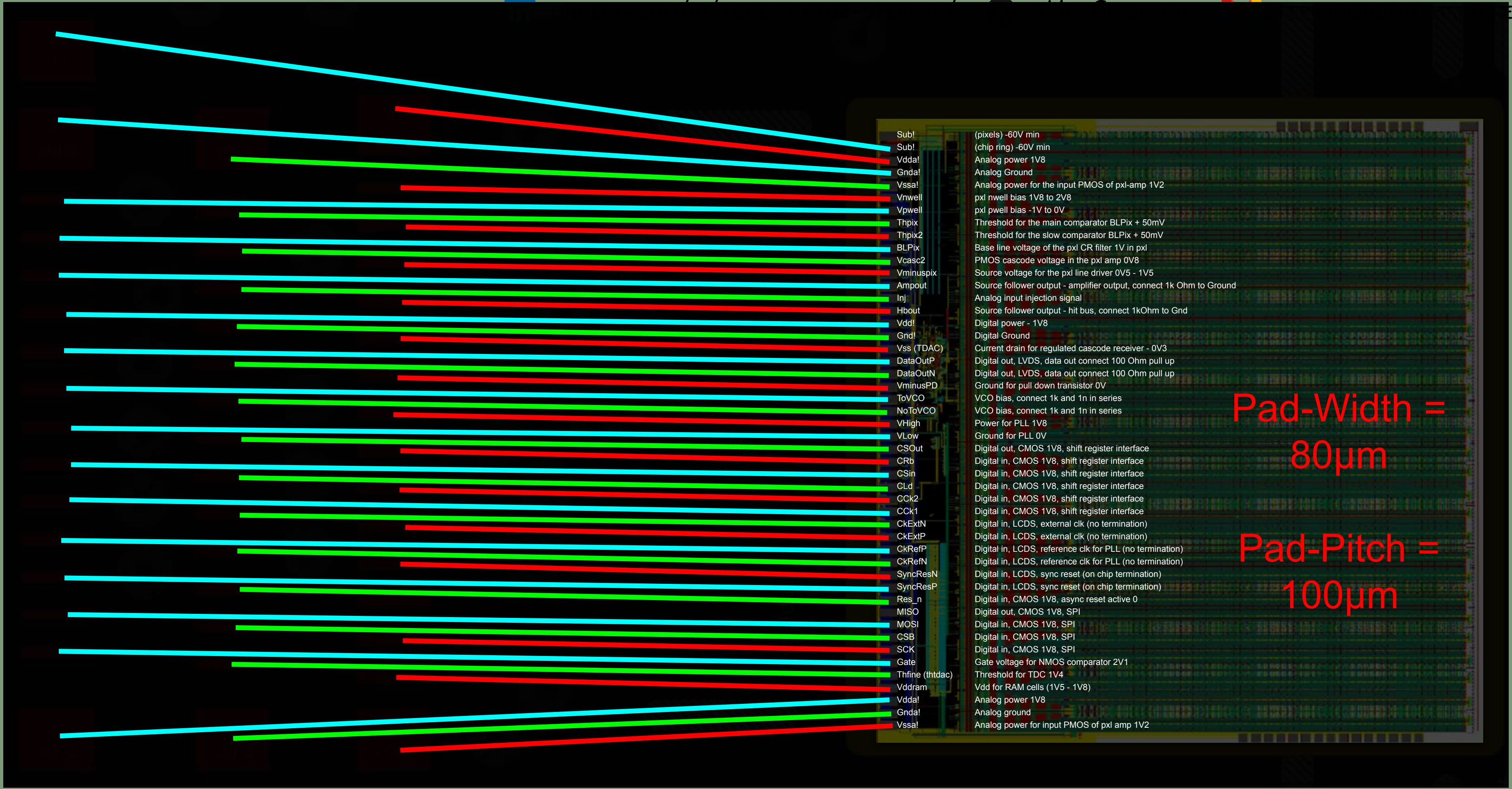
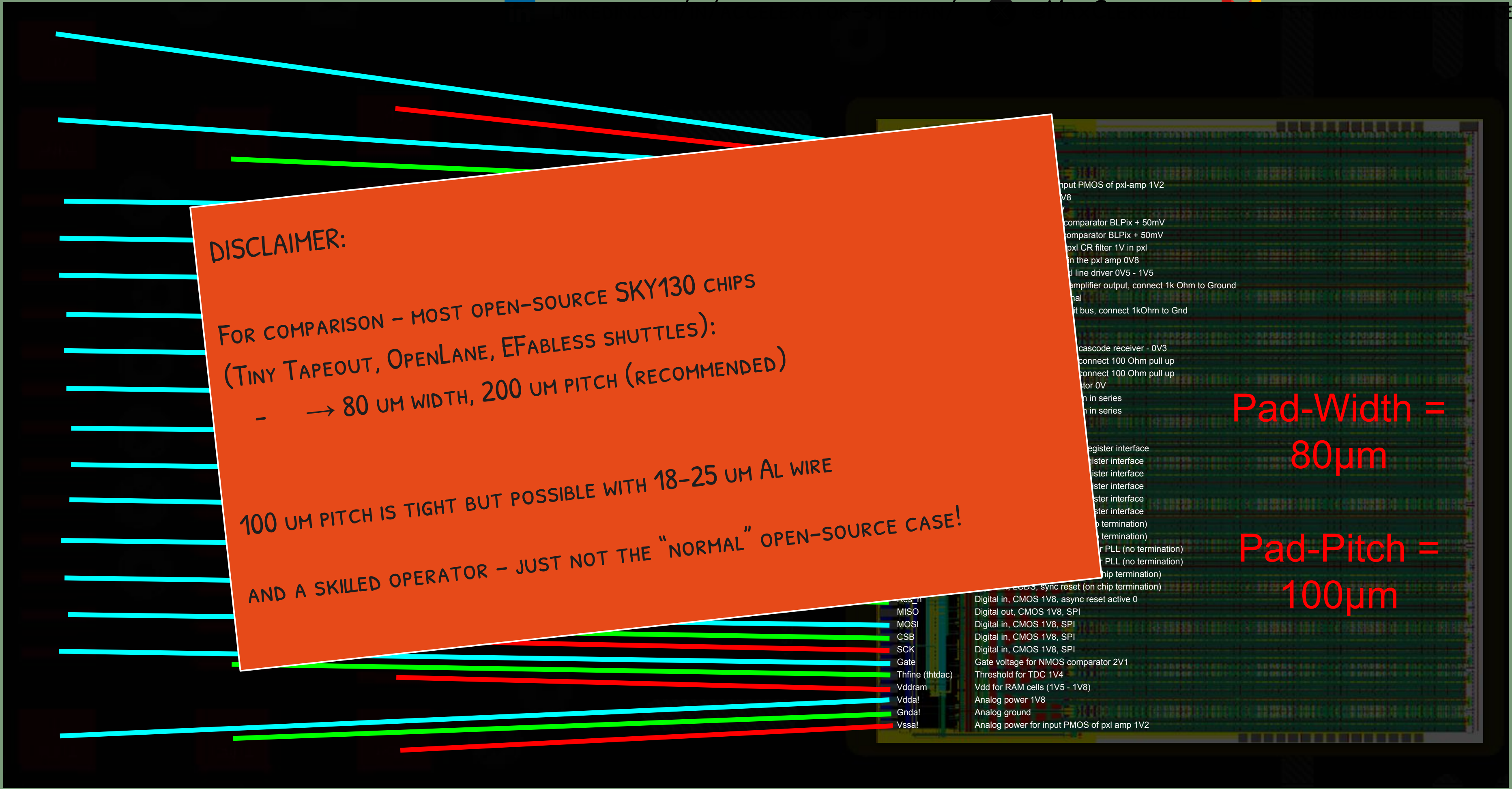

Sub! (pixels) -60V min
Sub! (chip ring) -60V min
Vdda! Analog power 1V8
Gnda! Analog Ground
Vssa! Analog power for the input PMOS of pxl-amp 1V2
Vnwell pxl nwell bias 1V8 to 2V8
Vpwell pxl pwell bias -1V to 0V
Thpix Threshold for the main comparator BLPix + 50mV
Thpix2 Threshold for the slow comparator BLPix + 50mV
BLPix Base line voltage of the pxl CR filter 1V in pxl
Vcasc2 PMOS cascode voltage in the pxl amp 0V8
Vminuspix Source voltage for the pxl line driver 0V5 - 1V5
Ampout Source follower output - amplifier output, connect 1k Ohm to Ground
Inj Analog input injection signal
Hbout Source follower output - hit bus, connect 1kOhm to Gnd
Vdd! Digital power - 1V8
Gnd! Digital Ground
Vss (TDAC) Current drain for regulated cascode receiver - 0V3
DataOutP Digital out, LVDS, data out connect 100 Ohm pull up
DataOutN Digital out, LVDS, data out connect 100 Ohm pull up
VminusPD Ground for pull down transistor 0V
ToVCO VCO bias, connect 1k and 1n in series
NoToVCO VCO bias, connect 1k and 1n in series
VHigh Power for PLL 1V8
VLow Ground for PLL 0V
CSOut Digital out, CMOS 1V8, shift register interface
CRb Digital in, CMOS 1V8, shift register interface
CSin Digital in, CMOS 1V8, shift register interface
CLd Digital in, CMOS 1V8, shift register interface
CCk2 Digital in, CMOS 1V8, shift register interface
CCk1 Digital in, CMOS 1V8, shift register interface
CkExtN Digital in, LCDS, external clk (no termination)
CkExtP Digital in, LCDS, external clk (no termination)
CkRefP Digital in, LCDS, reference clk for PLL (no termination)
CkRefN Digital in, LCDS, reference clk for PLL (no termination)
SyncResN Digital in, LCDS, sync reset (on chip termination)
SyncResP Digital in, LCDS, sync reset (on chip termination)
Res_n Digital in, CMOS 1V8, async reset active 0
MISO Digital out, CMOS 1V8, SPI
MOSI Digital in, CMOS 1V8, SPI
CSB Digital in, CMOS 1V8, SPI
SCK Digital in, CMOS 1V8, SPI
Gate Gate voltage for NMOS comparator 2V1
Thfine (thtdac) Threshold for TDC 1V4
Vddram Vdd for RAM cells (1V5 - 1V8)
Vdda! Analog power 1V8
Gnda! Analog ground
Vssa! Analog power for input PMOS of pxl amp 1V2
Pad-Width = 80µm
Pad-Pitch = 100µm


DISCLAIMER:
For comparison – most open-source SKY130 chips
(Tiny Tapeout, OpenLane, EFabless shuttles):
- → 80 um width, 200 um pitch (recommended)
100 um pitch is tight but possible with 18–25 um Al wire
and a skilled operator – just not the "normal" open-source case!
Pad-Width = 80µm
Pad-Pitch = 100µm
Digital in, CMOS 1V8, async reset active 0
MISO
Digital out, CMOS 1V8, SPI
MOSI
Digital in, CMOS 1V8, SPI
CSB
Digital in, CMOS 1V8, SPI
SCK
Digital in, CMOS 1V8, SPI
Gate
Gate voltage for NMOS comparator 2V1
Thfine (thtdac)
Threshold for TDC 1V4
Vddram
Vdd for RAM cells (1V5 - 1V8)
Vdda!
Analog power 1V8
Gnda!
Analog ground
Vssa!
Analog power for input PMOS of pxl amp 1V2

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Wire Bonding – Connecting chips to electrodes with fine wires

Ultrasonic wire-bonding = solid-state welding process
interconnect a fine metallic wire (Au, Al, Cu) to a bond pad.

The tool applies a force and transmits
US-vibrations to the wire-substrate interface.
US-energy induces localized plastic deformation and
scrubbing action that breaks up surface,
enabling direct metal-to-metal interdiffusion.

Non-thermoactivated ultrasonic wire-bonding works solely
through pressure and ultrasonic energy.
particularly for aluminum wire bonding to
gold metallization in temperature-sensitive devices.

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The Wire-Bonder

Upwards of $150k (new & CNC-programmable)

Used manual bonders starting as low as $25k

Cleanroom or Clean Room

Main ingredients

- CNC Computer (for automation)
- Visibility (Camera and Microscope)
- Wire-Feed
- Stage

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The Wire-Bonder

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Cleanroom or Clean Room

Main ingredients

- CNC Computer (for automation)
- Visibility (Camera and Microscope)
- Wire-Feed
- Stage
- Bond-Head + Bond-Tool

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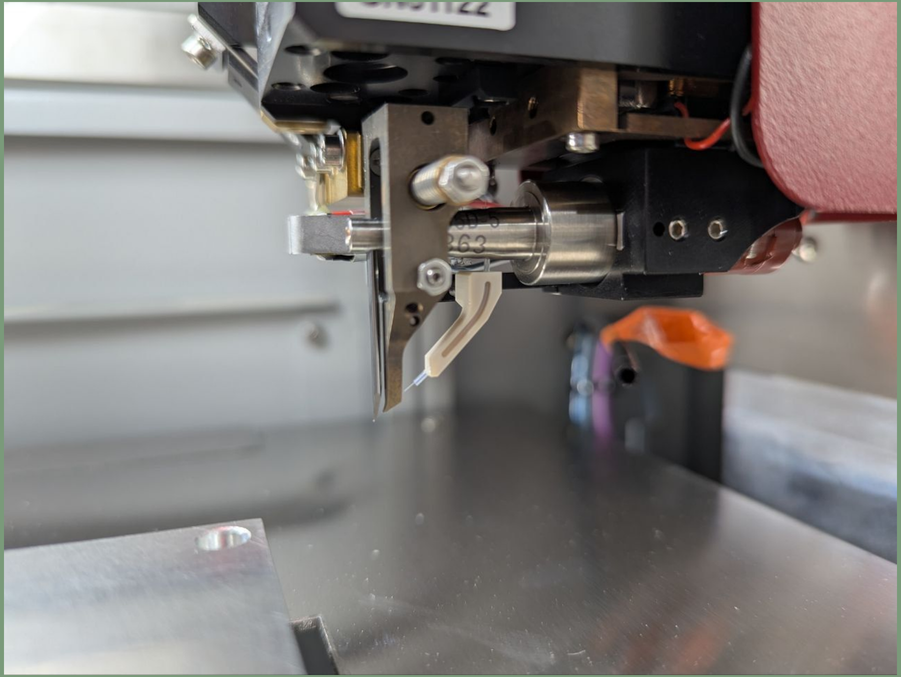
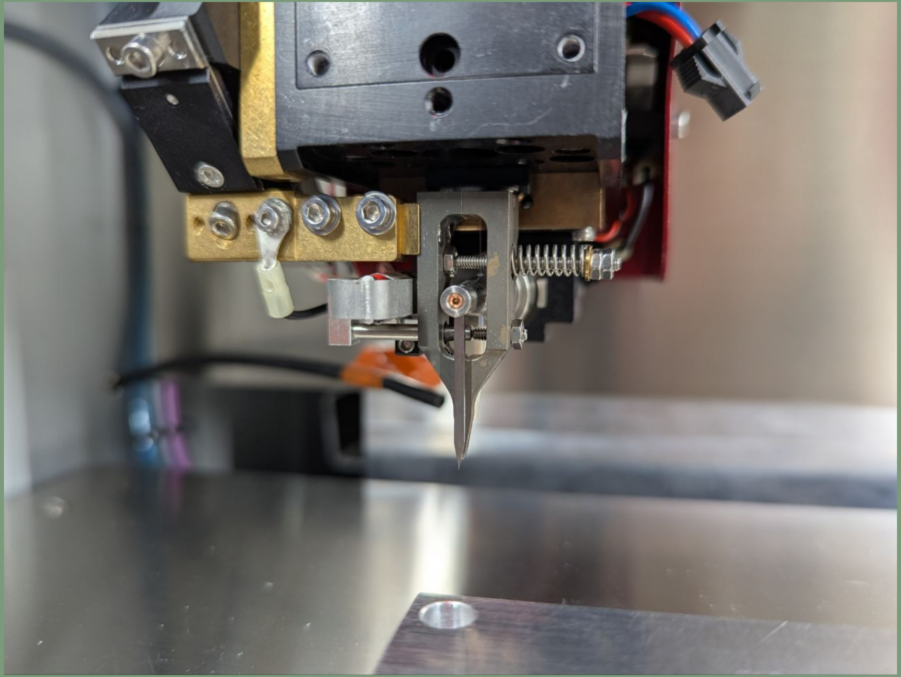
HEAD AND TOOL = WIRE-FEED + CLAMP + CAPILLARY + WEDGE





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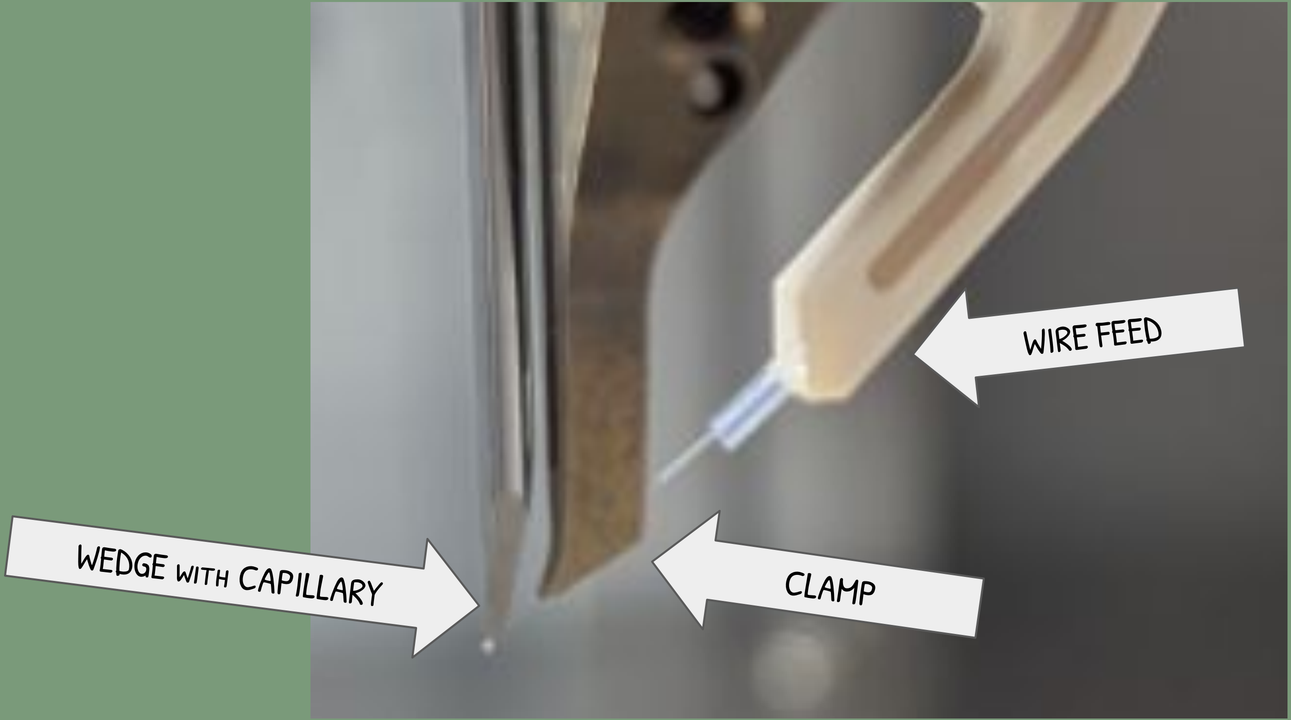
THE TOOL = WIRE-FEED + CLAMP + CAPILLARY + WEDGE



Better View of the Wedge

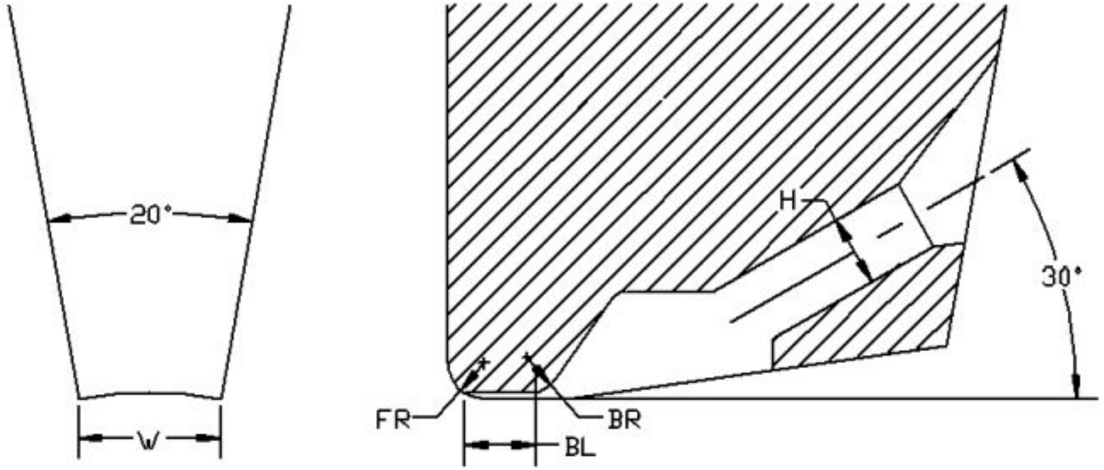


Figure 1: Schematic Diagram of the Wedge-shaped Capillary Cross-section.

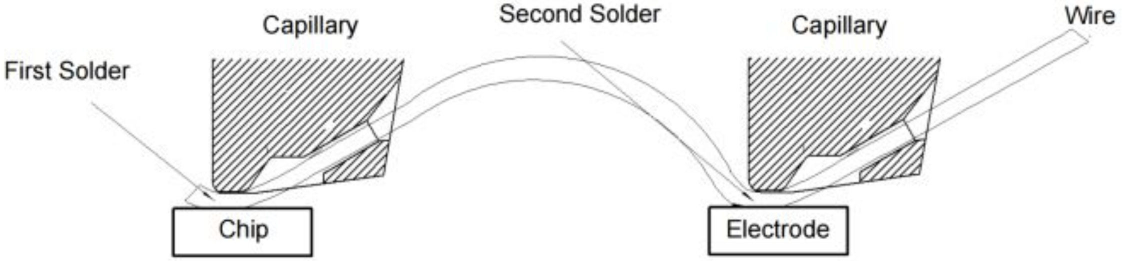


Figure 2: Schematic Diagram of Ultrasonic Wire Bonding.

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Initial Contact

Scrubbing

Deformation

Atomic Bonding / Interdiffusion

Intermetallic Compound

Tempering

Form the Loop

Same Again

Tear off

9 simple steps

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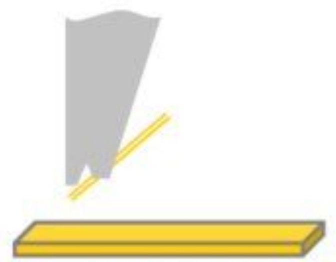
- Surface approaches.
- Electrodes position wire, substrate remains stable.
- Mechanical force establishes initial intimate contact.
- On contact: pressure builds, alignment begins.
- Energy focuses across minuscule bonding zone.
- Wire conforms, adapting to target surface.
- Foundation forms for subsequent metallurgical processes.



Approach for the 1st bond

(a)

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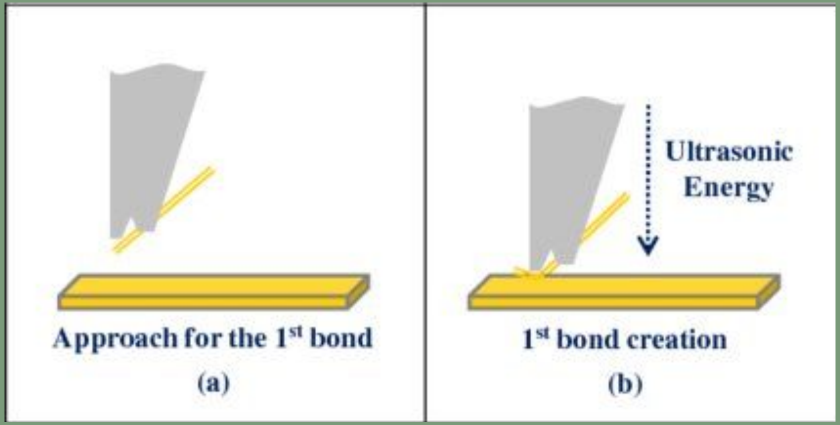
- Ultrasonic vibration initiates micro-scale scrubbing (60-140kHz).
- Localized relative motion disrupts residual interfacial barriers.
- removes oxides and contaminants.
- Surface asperities break, exposing clean metal.
- Frictional energy enhances atomic mobility significantly.
  - Introducing lattice defects
  - significant heat in attoliter volume (>800°C)
- Scrubbing establishes contact conditions reliably.



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Initial Contact

Scrubbing

Deformation

Atomic Bonding / Interdiffusion

Intermetallic Compound

Tempering

Form the Loop

Same Again

Tear off

- Applied force reshapes wire under stress.
- Plastic flow accommodates surface irregularities fully.
- Wire flattens, enlarging contact area gradually.
- Mechanical shaping supports stronger atomic coupling.
- Interfaces compress, reducing interfacial voids.
- Deformation prepares pathway for interdiffusion phenomena.

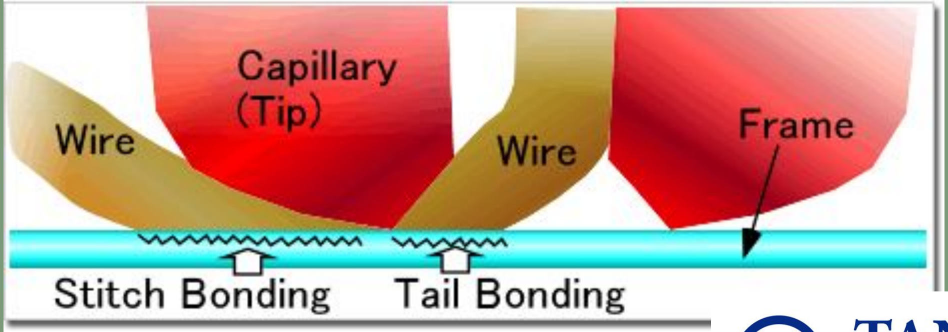

Fig.5

TANAKA
TANAKA PRECIOUS METALS

- Clean metallic atoms encounter neighboring atoms.
- Diffusion initiates across freshly activated interface.
- Atomic proximity allows electronic orbital overlap.
- Gradual interdiffusion integrates wire and pad.
- Metallurgical cohesion strengthens mechanical bond integrity.
- Atomic attraction consolidates irreversible metallurgical junction.

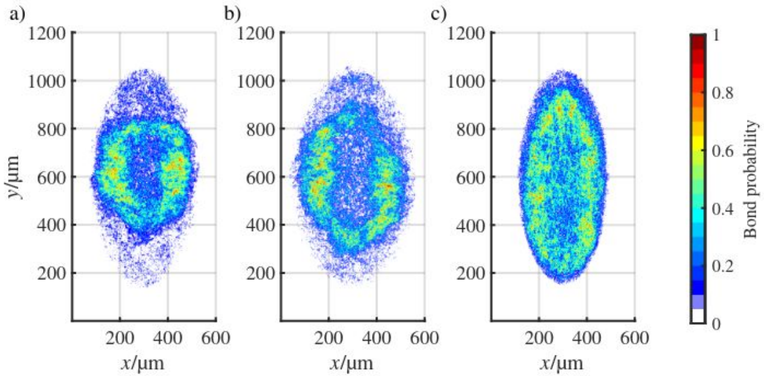

Figure 3.29: Results of image segmentation at 10.000 oscillation cycles of 15 pealed interface images for a) 37 kHz, b) 60 kHz and c) 100 kHz.

Schemmel, 2022

- Distinct phases form between contacting metals.
- IMC nucleate at bonding interface.
- Growth depends on temperature, time, chemistry.
- These compounds stabilize initial metallurgical connection.
- Excessive growth risks brittle joint formation.
- Controlled kinetics ensure reliable intermetallic structure.

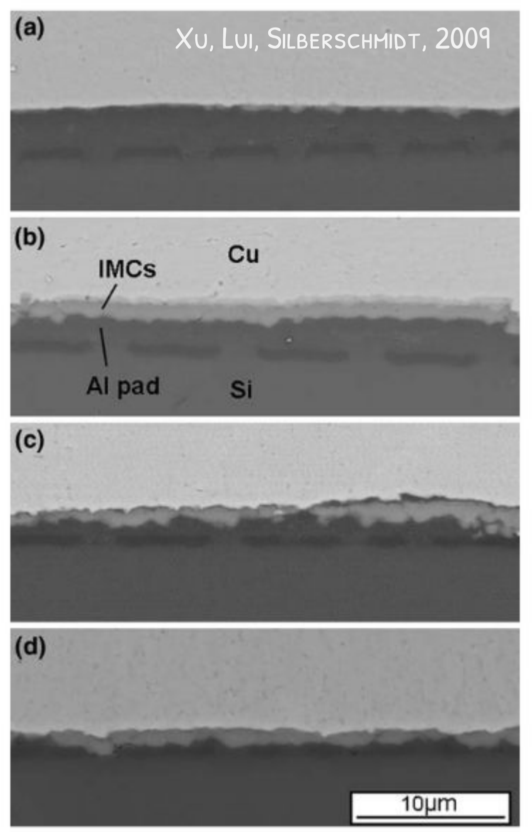

Fig. 6. Cross-sectional BSE SEM of copper ball/Al metallization interfaces after aging at 200°C for: (a) 1 day, very small IMCs formed; (b) 4 days, a layer of IMCs formed; (c) 64 days, thicker IMCs; and (d) 121 days, 1.5-μm-thick IMCs formed.

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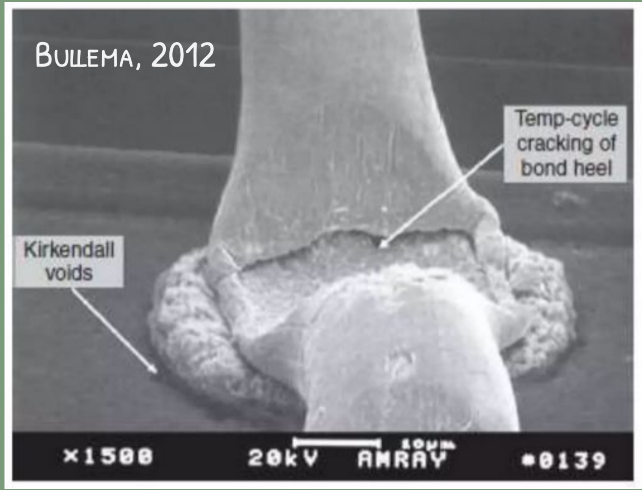
- Optional
- Bond undergoes stress relaxation through tempering.
- Residual mechanical strain gradually dissipates internally.
- Heat enhances microstructural stabilization post-bonding.
- Diffusion balances interfacial composition more uniformly.
- Bond achieves greater toughness and reliability.



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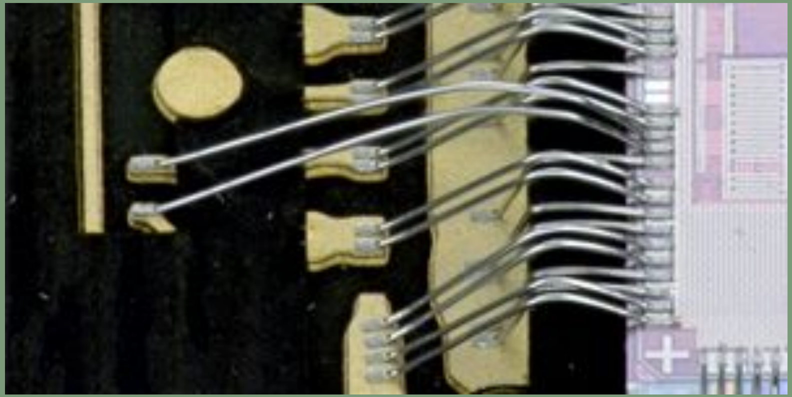
Initial Contact
Scrubbing
Deformation
Atomic Bonding / Interdiffusion
Intermetallic Compound
Tempering
Form the Loop
Same Again
Tear off

- Capillary ascends, wire follows guided trajectory.
- Loop height determined by programmed machine parameters.
- Ultrasonic vibrations cease during upward formation.
- Wire bends smoothly, defining electrical interconnect.
- Mechanical path optimizes stress distribution effectively.
- Loop geometry ensures functional electrical connection.



PALOMAR® TECHNOLOGIES

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- Bonding tool repositions for subsequent connection.
- Wire aligns with second substrate pad.
- Capillary descends, initiating another contact sequence.
- Ultrasonics and force replicate bonding cycle.
- Second metallurgical junction forms identically stable.
- Process repeats ensuring reliable electrical chain.

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- Capillary clamps wire securely near end.
- Upward motion applies tensile fracture force.
- Wire severs at predetermined weak point.
- Tail remains positioned for subsequent cycle.
- Tear-off completes wire bonding operation.

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Errors

1. Non-Stick on Pad (NSOP)
   - Wire fails to bond to pad
   - Causes: contamination, low force, low ultrasonics
   - Effect: open circuit, no electrical contact

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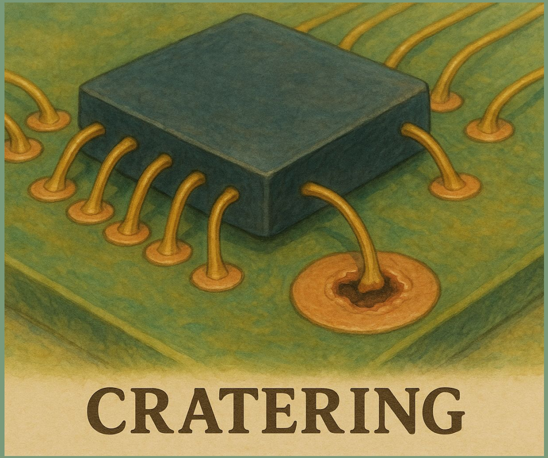
Errors

1. Non-Stick on Pad (NSOP)
   - Wire fails to bond to pad
   - Causes: contamination, low force, low ultrasonics
   - Effect: open circuit, no electrical contact

2. Cratering / Pad Damage
   - Pad metallization or silicon damaged
   - Causes: excessive force, power, or time
   - Effect: device damage, reduced yield, latent failure



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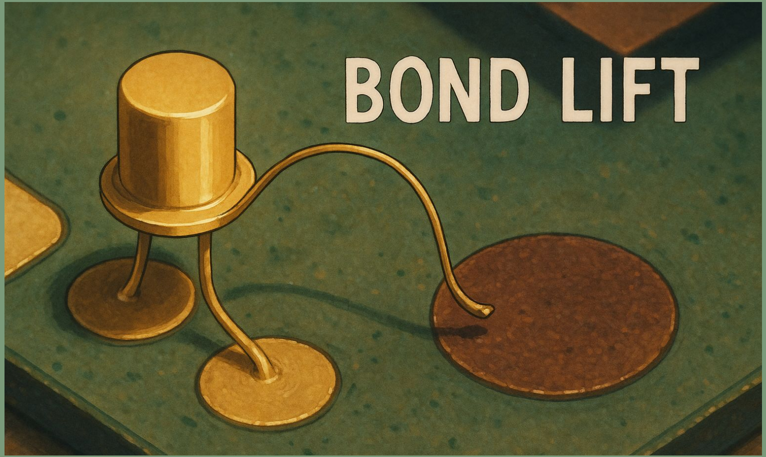
Errors



1. Non-Stick on Pad (NSOP)
   - Wire fails to bond to pad
   - Causes: contamination, low force, low ultrasonics
   - Effect: open circuit, no electrical contact

2. Cratering / Pad Damage
   - Pad metallization or silicon damaged
   - Causes: excessive force, power, or time
   - Effect: device damage, reduced yield, latent failure

3. Bond Lift
   - Bond forms but later detaches
   - Causes: short bond time, poor scrubbing
   - Effect: intermittent or unreliable connection

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Parameters: Bond Force

- Applied force presses wire against pad.
- Correct level ensures intimate surface contact.
- Too little causes incomplete mechanical deformation.
- Too much risks pad structural damage.
- Force control critical for consistent bond reliability.

Parameter	Too Low	Optimal	Too High
Bond Force	Non-stick on pad (NSOP)	Strong, reliable bond	Cratering, pad damage, excessive deformation

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Parameters: Ultrasonic Power

- Ultrasonic vibration supplies localized scrubbing energy.
- Amplitude determines oxide disruption and interdiffusion rate.
- Too low leads to weak adhesion.
- Excessive power damages wire or substrate.
- Power tuning depends on metallization and material.

Parameter	Too Low	Optimal	Too High
Bond Force	Non-stick on pad (NSOP)	Strong, reliable bond	Cratering, pad damage, excessive deformation
Ultrasonic Power	Weak bond, poor scrubbing, NSOP	Proper oxide removal, stable bond	Wire necking, pad damage, cratering

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Parameters: Bond Time

- Duration defines exposure to energy input.
- Short time produces insufficient atomic bonding.
- Extended time risks brittle intermetallic formation.
- Careful control ensures optimal joint microstructure.
- Time interacts closely with force and power.
- Precise timing secures repeatable bonding quality.

Parameter	Too Low	Optimal	Too High
Bond Force	Non-stick on pad (NSOP)	Strong, reliable bond	Cratering, pad damage, excessive deformation
Ultrasonic Power	Weak bond, poor scrubbing, NSOP	Proper oxide removal, stable bond	Wire necking, pad damage, cratering
Bond Time	Incomplete bond, bond lift	Sufficient interdiffusion, strong bond	Brittle IMCs, pad damage, cratering

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Parameters: Surface Cleanliness

- Surface oxides and contaminants hinder bonding.
- Scrubbing exposes fresh reactive metal layers.
- Clean pads maximize ultrasonic efficiency significantly.
- Contamination leads to unreliable weak connections.
- Wire and pad preparation is critical.
- Surface integrity dictates final bond performance.

Parameter	Too Low	Optimal	Too High
Bond Force	Non-stick on pad (NSOP)	Strong, reliable bond	Cratering, pad damage, excessive deformation
Ultrasonic Power	Weak bond, poor scrubbing, NSOP	Proper oxide removal, stable bond	Wire necking, pad damage, cratering
Bond Time	Incomplete bond, bond lift	Sufficient interdiffusion, strong bond	Brittle IMCs, pad damage, cratering
Surface Cleanliness	NSOP, bond lift, poor adhesion	Clean contact, strong atomic bond	– (excess cleanliness has no drawback)

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THE BOND PLACEMENT

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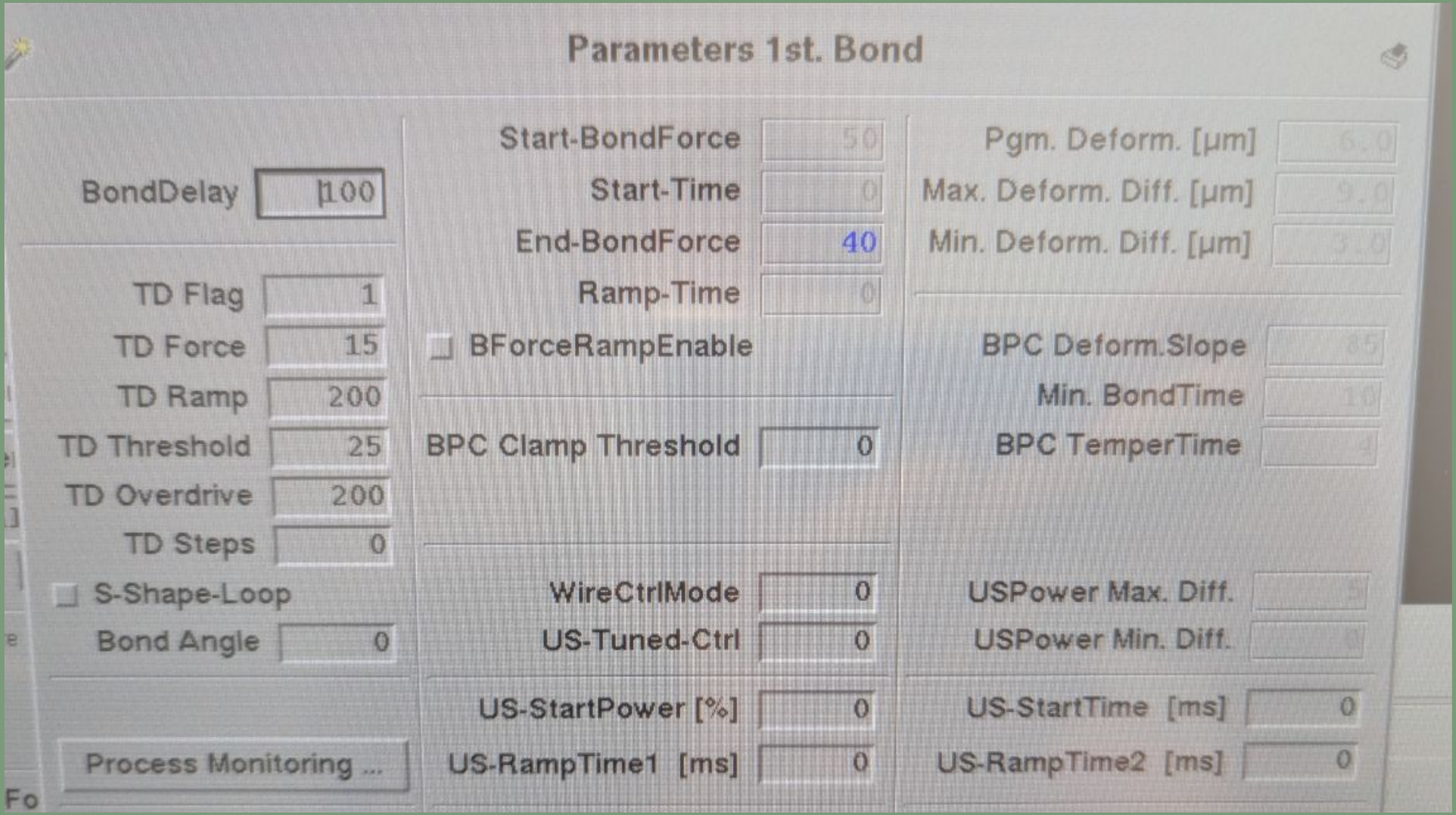
The Bond Parameters



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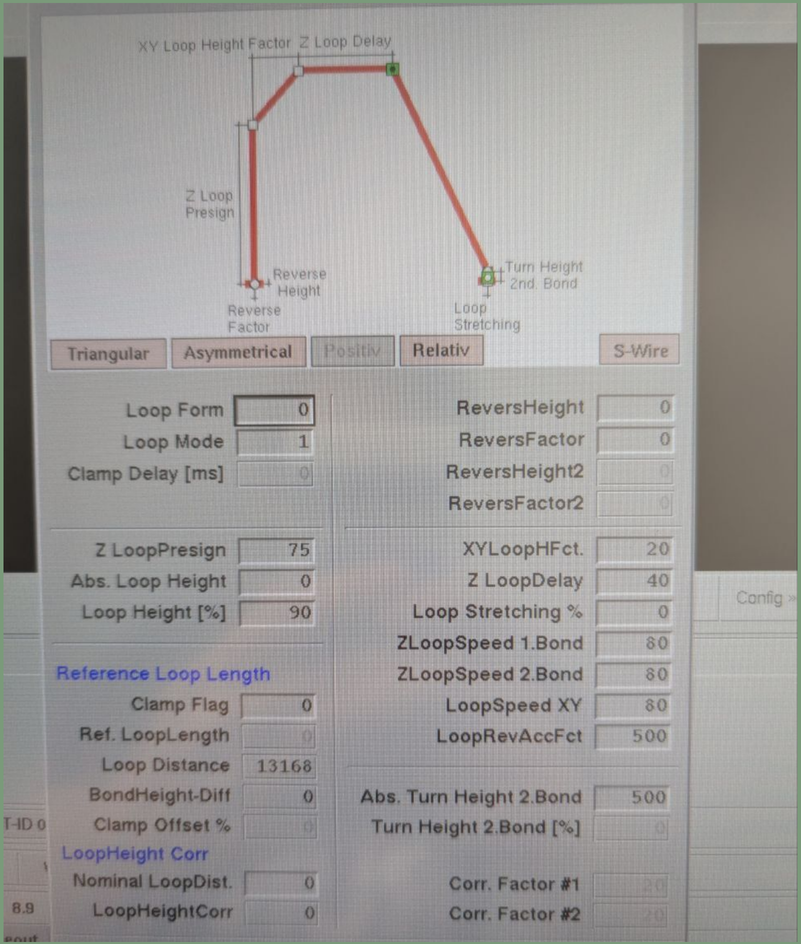
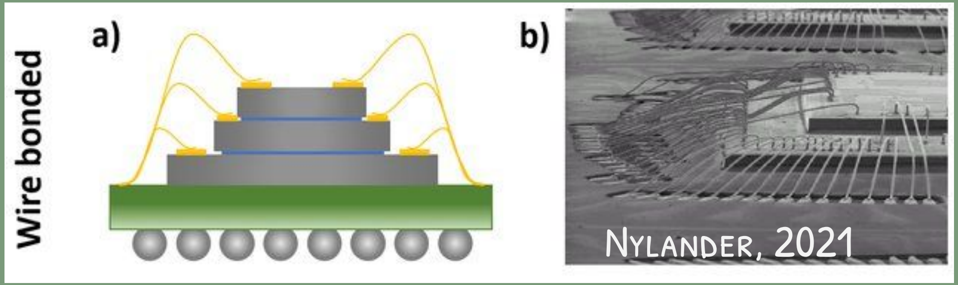
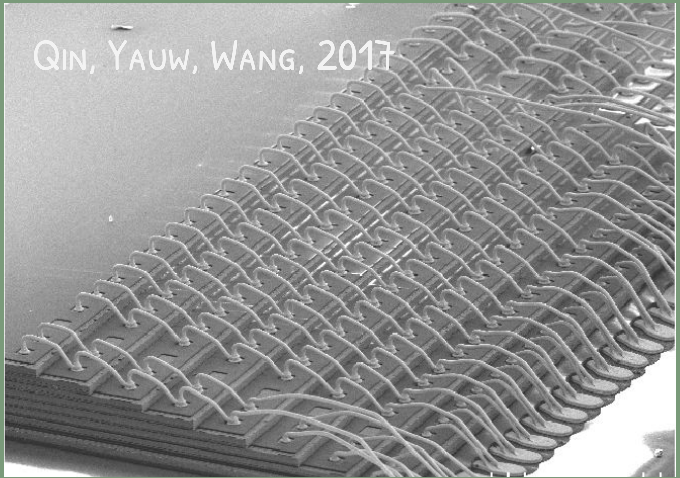


The Loop Parameters

Adjust the trajectory the bond head should perform between first and second bond





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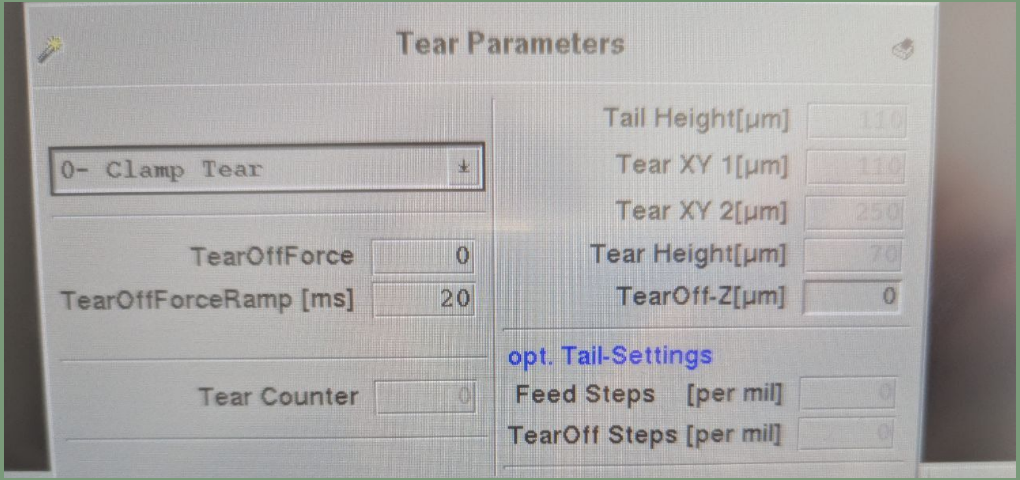
The Tear Parameters



Configure how the wire should be torn off after the second bond

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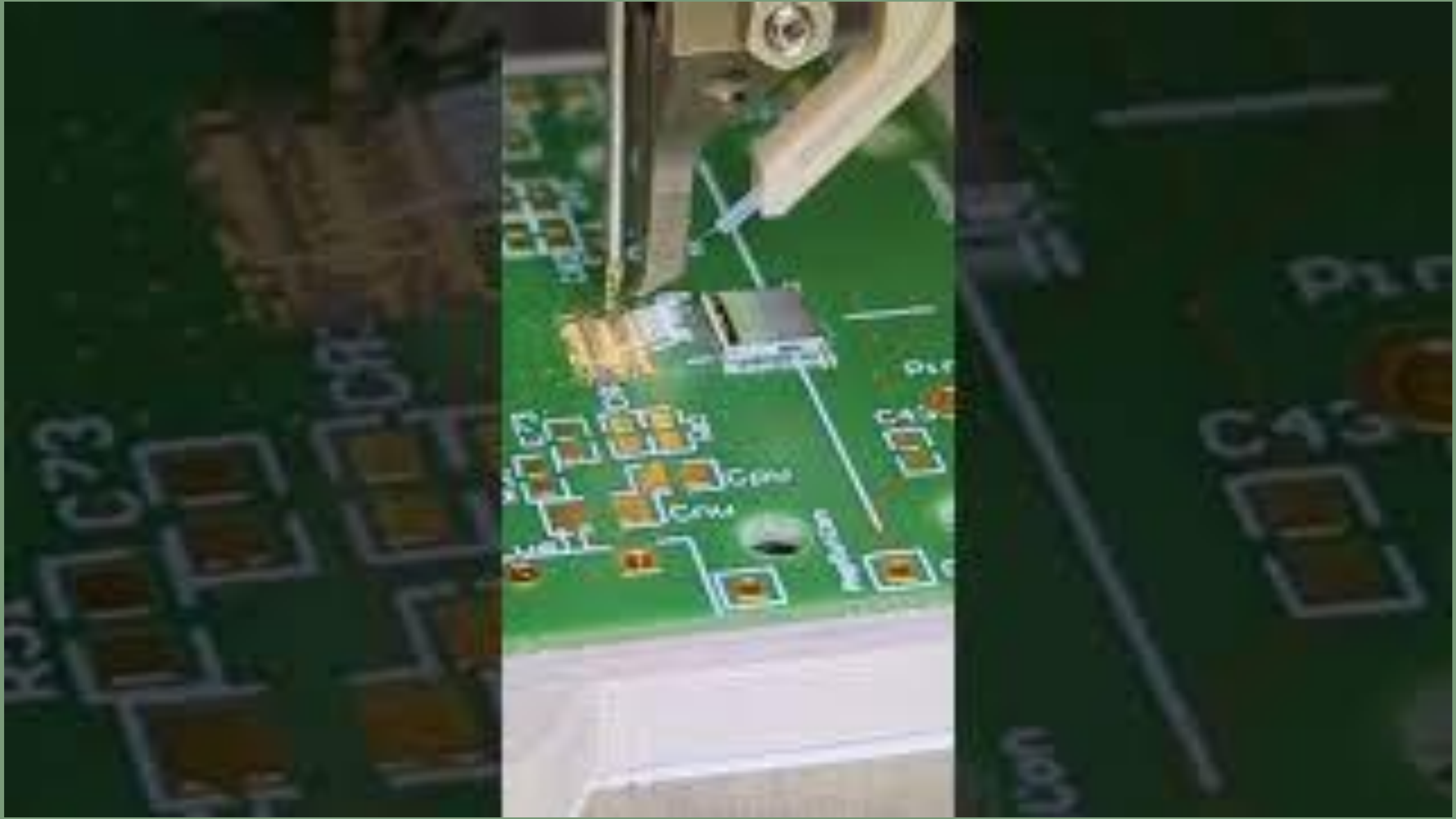

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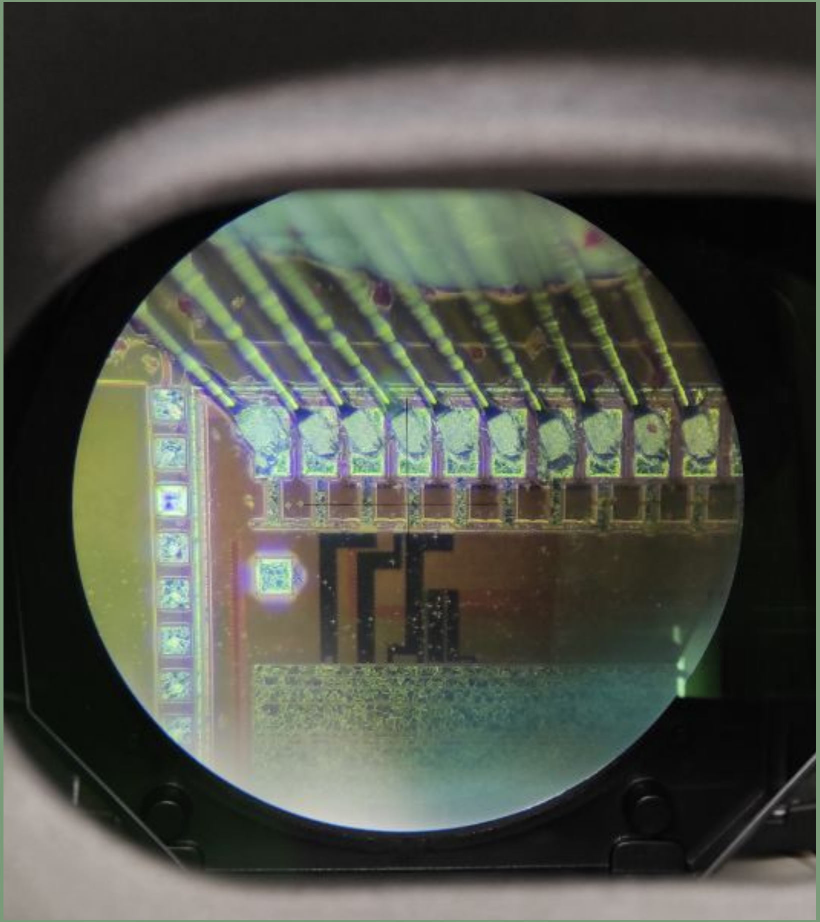

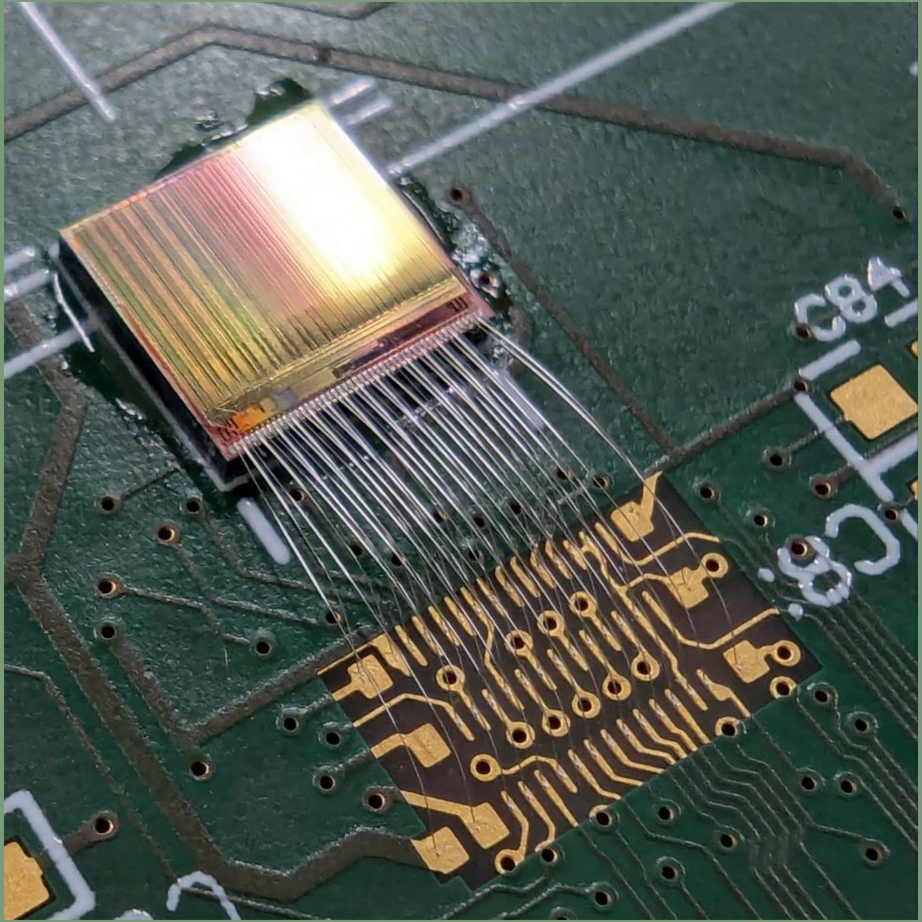

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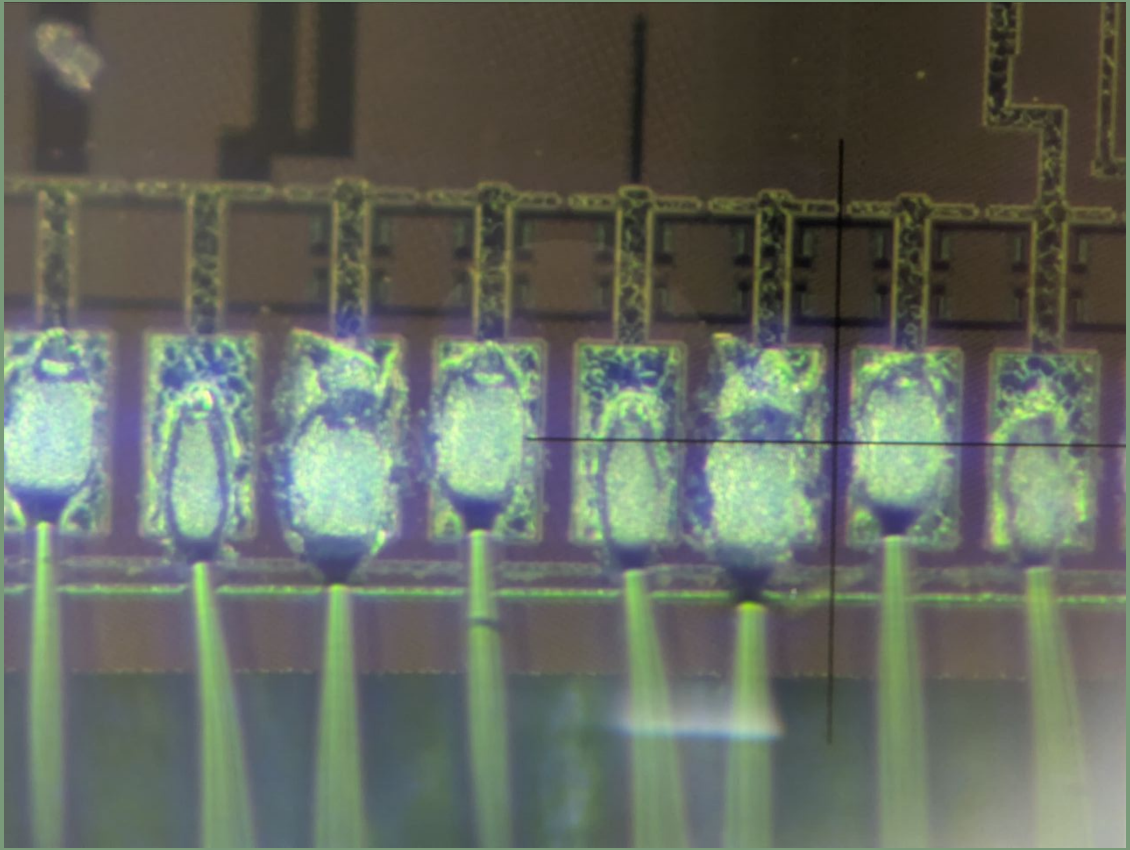

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My Summary

- Hardware is hard
- 1960 – this was done by hand
- it became big-industry tech
- 2030 – 3D-printer like?
- How does this relate to open source PCB and chip design?
- What does that mean in the future?

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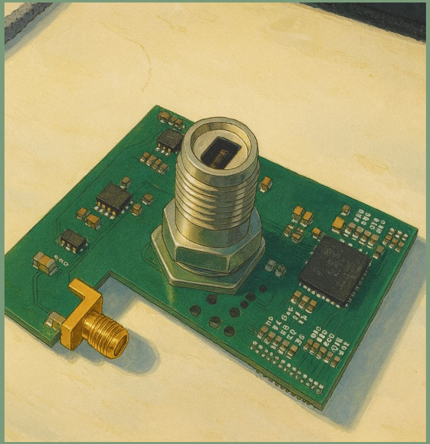

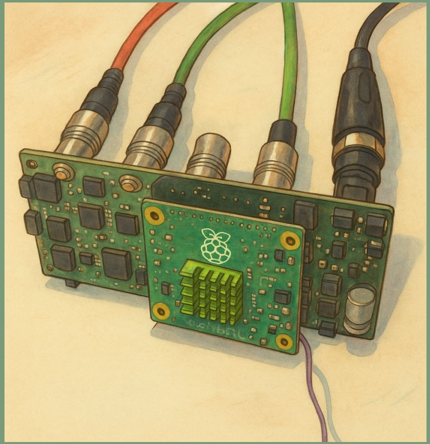

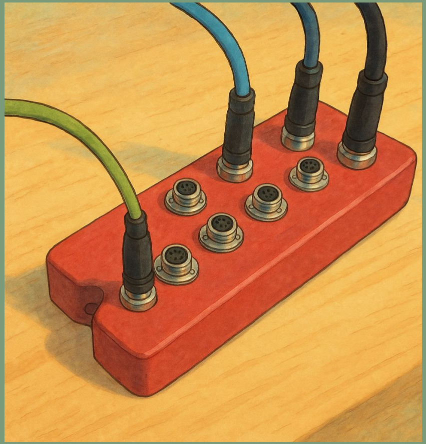

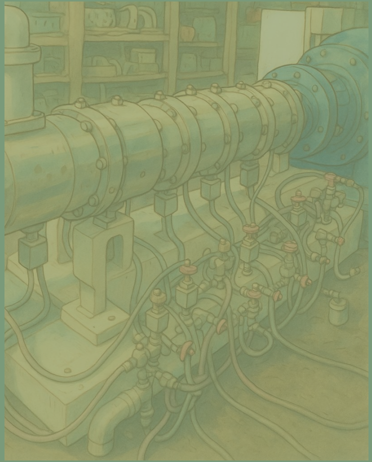

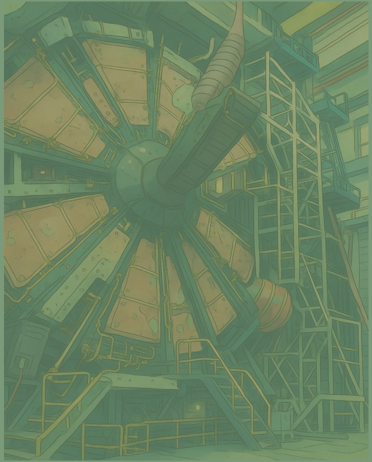

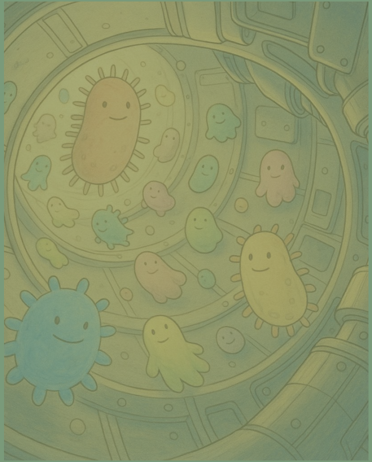

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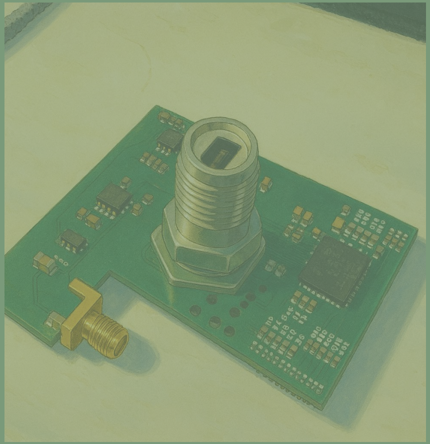
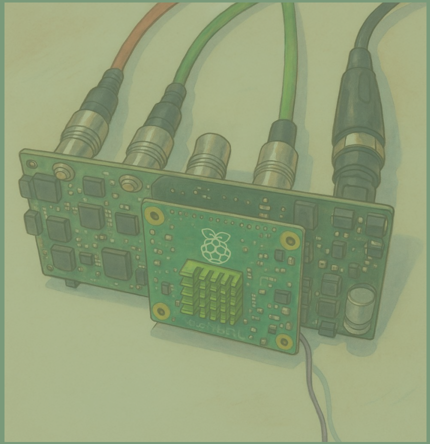
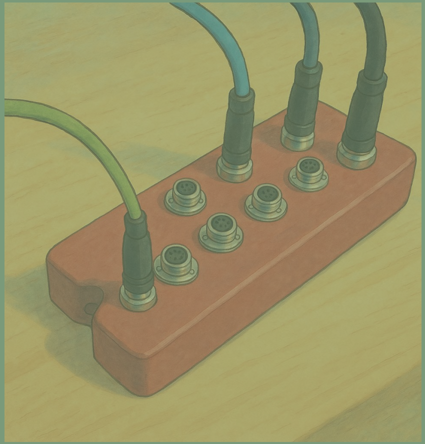

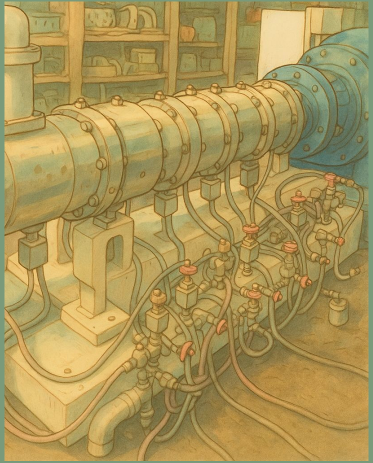
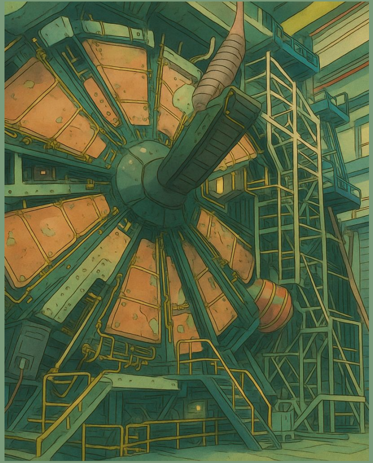


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